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EXAMINER	
ARCOS, CAROLINE H	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/733,174	OKA ET AL.
	Examiner	Art Unit
	CAROLINE ARCOS	2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2011*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)	
1) ☐ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amendment filed on 03/03/2011.

2. Claims 1-10 and 12-13 are pending for examination. Claims 1 and 7 are independent claims. In the amendment claim 11 has been cancelled. This action is made final.

Claim Objections

3. Claim13 is objected to because of the following informalities:

the claim contains grammatical mistake. The claim need to replace " are" in the second line with "is" since the claim is addressing each processor

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki et al. (Us 2002/0138707 A1).

5. Suzuoki et al. (Us 2002/0138707 A1) was cited in the previous office action dated 11/10/2010.

6. As per claim 1, Suzuoki teaches the invention substantially as claimed including a signal processing device, comprising:

a general-purpose signal processor formed of a plurality of component-processors, each of the component-processors operates in parallel under a plurality of configurations of connections of the plurality of component-processors associated with a plurality of software tasks, and operating independently from other component-processors (par. [0012-0014]; par. [0018]; par. [0058]; par. [0131-0139] defines different configuration; wherein PE is general purpose signal processor and APUs are the component-processors); and

a management processor for selecting a number of component-processors to operate and for configuring the connections of the plurality of operating component-processors and for assigning and loading application programs into the component-processors in response to a demand for signal processing calculated based on a type of processing and an estimated load of an entire processing (par. [0012-0014]; par. [0017-0019]; par. [0021]; par. [0065]; par. [0123]; par. [0126]; wherein PU is the management processor that orchestrates the processing of applications by the APUs and assigning and loading applications to the APUs based on the demand of signal ' application processing' that is based on the amount of processing capability needed and type of application such as

steaming application).

7. Suzuoki does not explicitly teach each of the component-processor executes only an assigned application until another demand for signal processing is received.

8. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Suzuoki teaching of PU schedules and orchestrate the processing of application by APUs, the PU control the APU by issuing direct memory access commands to the DMAC which controls the accesses to the applications stored in the shared DRAM. Hence, each of the component-processor executes only an assigned application until another demand for signal processing is received as claimed.

9. As per claim 2, Suzuoki teaches an input/output interface for receiving a signal to be processed inputted from an external device or one of the component-processors, and for outputting a processed signal to the external device or one of the component-processors, wherein the management processor controls the input/output interface so as to swap one of the component-processors which receives the signal to be processed which is inputted through the input/output interface or outputs the processed signal in accordance with a demand for signal processing (Par. [0067]; Par. [0072]; Par. [0074]; Par. [0110]; Par. [0131]-Par. [0139]; wherein the PU orchestrates and control the processing of data and application by APU and Controlling which APU does what task by grouping the

APUs based on the type of signals).

10. As per claim 3, Suzuoki teaches the input/output interface includes a cross bus switch that can selectively connect, under the control of the management processor, the external device to one of the component-processors, or the component-processors to each other (fig. 3, 317, 311; Par. [0018]; Par. [0065]; Par. [0067]; Par. [0072]).

11. As per claim 4, Suzuoki teaches the input/output interface includes a multiple bus that can selectively connect, under the control of the management processor, the external device to one of the component-processors, or the component-processors to each other (fig. 3, 317, 31 l; par. [0018]; par. [0065]; par. [0067]; par. [0072]).

12. As per claim 5, Suzuoki teaches wherein a local memory is disposed on each of the component-processors, said local memory stores a signal to be processed or a signal processed result by the component-processors until the signal to be processed or the signal processed result becomes available to be outputted to the input/output interface (par.[0064]; Par. [0083]; par. [0089]; Par. [0093]-Par. [0094]; Par. [0097]; Par. [0099]-Par. [0106]; Par. [0110]; Par. [0138]).

13. As per claim 6, Suzuoki teaches the general-purpose signal processor, the management processor and the input/output interface are disposed on one system (fig.3, element 319, 317, 303), the system including a first connection interface

being connectable to a device that provides a demand for signal processing to the management processor, and a second connection interface being connectable to the external device that delivers a signal with respect to the input/output interface (par. [0110]-par. [0111]).

14. Suzuoki does not explicitly teach that the system is a single case.

15. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that is well known that disposing the system on a single case is a design choice that enables the portability of the system.

16. As per claim 7, Suzuoki teaches an entertainment device, comprising:

a signal processing device including a general-purpose signal processor, a management processor, and an input/output interface (Fig. 3, elements 371,303); and

a main processor that provides a demand for signal processing to the signal processing device (par. [0066]; wherein the BE is the main processor; fig. 3, element 301), wherein the general-purpose signal processor is formed of a plurality of component-processors, each of the component-processors operates in parallel under a plurality of operating configurations of connections of the plurality of component-processors associated with software tasks and independently from other component-processors(par. [0012-0014]; par. [0017-0019]; par. [0021]; par. [0131-0139] defines different configuration; par. [0065];

par. [0123]; par. [0126]; wherein PE comprises a PU, DMAC and a plurality of APUs. The PU is the management processor that orchestrates the processing of applications by the APUs and assigning and loading applications to the APUs based on the demand of signal that is based on the amount of processing capability needed and type of task such as steaming application); and

the input/output interface inputs a signal to be processed from an external device or one of the component-processors, and outputs a processed signal to the external device or one of the component-processors (par. [0067]; par. [0072]; par. [0074]; par. [0087]; par. [0110]),

the management processor selects a number of component-processors to operate and configures the connections of the plurality of component-processors for assigning and loading application programs into the component-processors in response to the demand for signal processing provided from the main processor (par. [0012]- Par. [0014]; par. [0017]- Par. [0019]; par. [0021]; par. [0065]; par. [0123]; par. [0126]; wherein PU is the management processor that orchestrates the processing of data and applications by the APUs);

the demand for signal processing is estimated based on a type of processing and an estimated load of an entire processing (par. [0012]; par. [0014]; par. [0019]; Par. [0131]; par. [0065]),

controls the input/output interface so as to swap one of the component-processors which receives the signal to be processed which is inputted through the input/output interface or outputs the processed signal in accordance with the demand for signal processing(par. [0067]; par. [0072]; par. [0074]; par. [0110];

par. [0131-0139]; wherein the PU orchestrates and control the processing of data and application by APU and Controlling which APU does what task by grouping the APUs based on the type of signals).

17. Suzuoki does not explicitly teach each of the component-processor executes only an assigned application until another demand for signal processing is received.

18. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Suzuoki teaching of PU schedules and orchestrate the processing of application by APUs, the PU control the APU by issuing direct memory access commands to the DMAC which controls the accesses to the applications stored in the shared DRAM. Hence, each of the component-processor executes only an assigned application until another demand for signal processing is received as claimed.

19. As per claim 8, Suzuoki teaches a network interface that enables a connection with a computer network, and a storage means that stores digital information readable by a computer, wherein the main processor controls the network interface to acquire the digital information from an external device, stores the acquired digital information in the storage means, and provides the stored digital information and a demand for signal processing based on the digital information to the management processor of the signal processing device to constitute operating environments for entertainment processing the contents of which are

determined in accordance with the digital information (par. [0012-0013]; par. [0056-0057]; par. [0083]; par. [0085]; par. [0110]; par. [0120]; par. [0126]; par. [0131-0139]; wherein it is implicit that the system has a network interface wherein, the computers and the computer devices are connected to network and communicate with each other for processing data and application. Hence, there must be a network interface for these computers to communicate with each other).

20. As per claim 9, Suzuoki teaches the main processor constructs the operating environments for entertainment processing on one or more of the component-processors through the management processor, and, after constructing the operating environments, said main processor reconstructs said operating environments to new operating environments upon receipt of another digital information which differs from said digital information (par. [0013-0014]; par. [0018]; par. [0066]; par. [0082-0083]; par. [0131-0139] defines different configuration).

21. As per claim 10, Suzuoki teaches the digital information comprises plural kinds of application programs that can execute required functions, respectively, and wherein the management processor assigns any of the functions to the corresponding component-processors, and reads a corresponding application program for executing the assigned function from the storage means, and executes the application program(par. [0013-0014]; par. [0018]; par. [0066]; par. [0082-

0083]; par. [0131-0139] defines different configuration).

22. As per claim 12, Suzuoki teaches wherein each of the plurality of component-processors is formed of the same hardware structure (par. [0011-0012]; par. [0057]).

23. As per claim 13, Suzuoki teaches wherein each of the plurality of component-processors is formed of the same hardware structure (par. [0011-0012]; par. [0057]).

Response to Arguments

24. Applicant's arguments filed on 03/03/2011 have been fully considered but they are not persuasive.

25. Applicant argues the following:

    a. Suzuoki is silent regarding "Loading application programs into the component-processors in response to a demand for signal processing calculated based on a type of processing and an estimated load of an entire processing".

    b. Suzuoki is silent regarding "each of the component processors execute only an assigned application program until another demand for signal processing is received".

26. The examiner respectfully disagrees with the applicant in the following:

a. Regarding point "a", Suzuoki teaches each 'PE' comprises a 'PU', a DMAC and a plurality of 'APUs'. Each 'PE' has preferably eight 'APUs', greater or less depending on the processing power needed by the applications (entire load), a dedicated pipelined can be created for processing streaming data (type of processing). Each PU schedules and orchestrates the processing of the applications by the APUs. Suzuoki teaches that the 'APUs' do not directly access the DRAM where the application are stored. The software cells containing the applications are processed directly by the 'APUs' from the 'APUs" local storage. The 'PU' controls the 'APUs' by issuing direct memory access commands to the DMAC. The applications in the DRAM are read into the 'APUs' local storage before the 'APUs' process the application (loading the applications into the component processors). Hence, Suzuoki teaches loading application programs into the component-processors in response to a demand for signal processing calculated based on a type of processing and an estimated load of an entire processing as claimed (par. [0012-0013; 0065; 0120; 0131].

b. According to point 'b', Suzuoki does not explicitly teach each of the component-processor executes only an assigned application until another demand for signal processing is received. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Suzuoki teaching of PU schedules and orchestrate

the processing of application by APUs, the PU control the APU by issuing direct memory access commands to the DMAC which controls the accesses to the applications stored in the shared DRAM. Hence, each of the component-processor executes only an assigned application until another demand for signal processing is received as claimed (par. [0012-0013; 0065; 0120; 0131].

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

29. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the

mailing date of this final action.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 8:00 AM to 2:00 PM.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Caroline Arcos/
Examiner, Art Unit 2195

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195